JAVELIN ASIC DEVICES

WHITE PAPER

Seven Steps to a Successful Analog ASIC

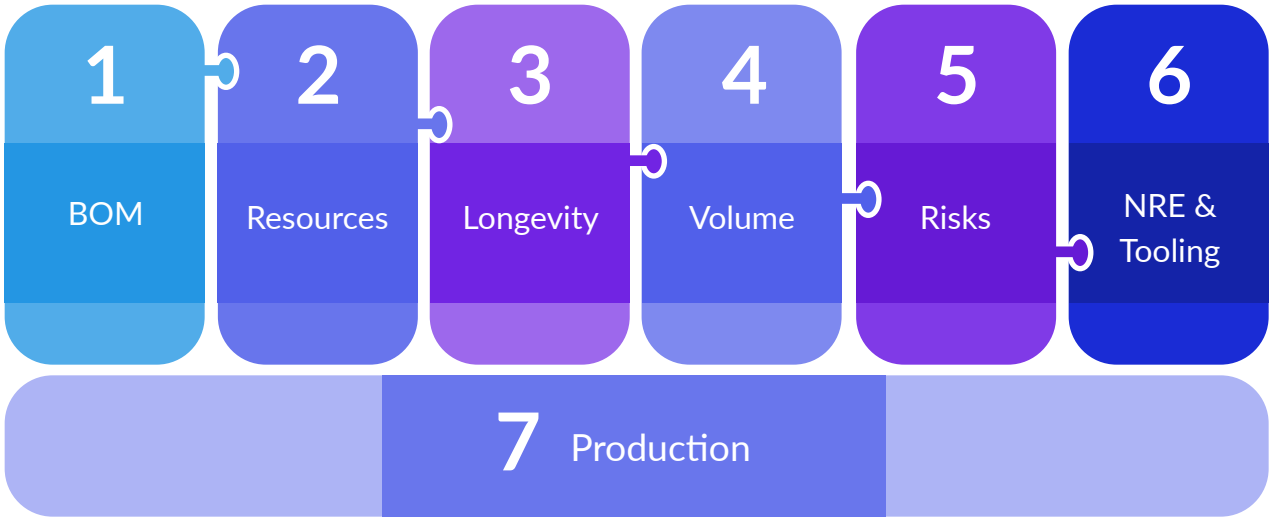
— Bob Frostholm —

I'm willing to bet that there are tens of thousands of analog applications out there that would benefit financially from ASIC integration. So what's the holdup? Based on my 50+ years in the analog IC business, I can boil it down to one word: misinformation. It's high time we dispel the myths surrounding analog ASIC integration and expose the bare-bones truth — most of the time, it's the sensible thing to do. However, confusion concerning the preparatory steps leading up to a proposal for non-recurring engineering (NRE) and tooling is often an early show-stopper.

Proper planning in anticipation of having an analog ASIC developed and produced for your company is essential. There are six key elements you need to explore internally before engaging a semiconductor company to design and produce a custom chip for you.

Once you are comfortable with this internal analysis, you can then explore possible suppliers. If you've done the internal analysis correctly, you will have realized that there is much more to NRE than the upfront costs for designing and tooling a custom chip. That's the easy part, because it's spelled out clearly in the contract you'll be signing at the beginning of the project. However, there's a hidden part of NRE that few companies successfully quantify. And for good reason — it's not easy. Let's take a moment to examine some of the more important aspects before going into production and development.

There are several pieces to the ASIC puzzle, and they must all fit together before a proper decision to move forward can be made.



1 BOM

Identify your existing BOM costs. When asked, most customers simply get a list of components and their cost from the purchasing department. Less obvious are the other costs associated with these components, such as purchasing, inventory, manufacturing (including human and machine labor), cost per square inch of the PCB, and lost production due to supplier availability or quality issues. This last one is especially difficult to financially quantify. Furthermore, there are also BOM costs associated with an ASIC. A new PCB layout is required and additional qualification and reliability testing may be involved. All of these costs need to be scrutinized closely when considering a move to an ASIC solution. Before committing, be sure to quantify all the costs you will incur against those you will be saving.

2 Resources

Identify your available resources for managing the transition to a single ASIC. Someone in your organization needs to serve as the point person with the ASIC company, fielding technical questions, defining electrical specifications, conducting progress and design reviews, overseeing the production change-over, and more. This role will carry a lot of responsibility, so be sure to select someone capable of shouldering it and have a backup plan in case they leave in the future.

3

Longevity

Understand the longevity and cumulative volume expectations for your product. There's not much point in undertaking the effort to develop an ASIC if its lifespan is too short. There are, of course, obvious exceptions, such as applications in which the volumes are vast, like mobile phones and computers. In these products, even if the lifetime of a chip is only a couple of years, the savings clearly justify the transition. Fortunately, analog applications typically have long lifespans and can easily support and justify the transition to an ASIC chip. For example, many industrial and medical applications can last 10 years or longer.

4

Volume

Don't overestimate your volume expectations to try to lure an ASIC supplier; it's always better to err on the conservative side and underestimate. The fact is, analog ASICs do not require high volumes. While everyone's definition of "high volume" varies, to quantify it, many projects are successful at 25-50K units per year, sometimes less. Analog ASICs have always been affordable, and the perception that they aren't is perhaps the single biggest misconception about them.

5

Risks

While it is your responsibility to manage the four puzzle pieces discussed above, the fifth piece — mitigating risks — is shared by you and your supplier. The risks associated with ASIC development must be analyzed on both sides. What if your volume expectations aren't realized? What if your analog ASIC supplier is unable to meet the completion date? Or worse yet (and all too common) what if you select a supplier that doesn't have the skill set to complete the job and meet all your technical requirements? Asking for last-minute waivers can kill your entire project, but you can avoid this by investing in advanced research. Javelin, for example, always performs a feasibility study before engaging in a development contract. In addition, you should check references and speak to the leader of the ASIC design team to assess their skills and understanding of both analog chip design and your application.

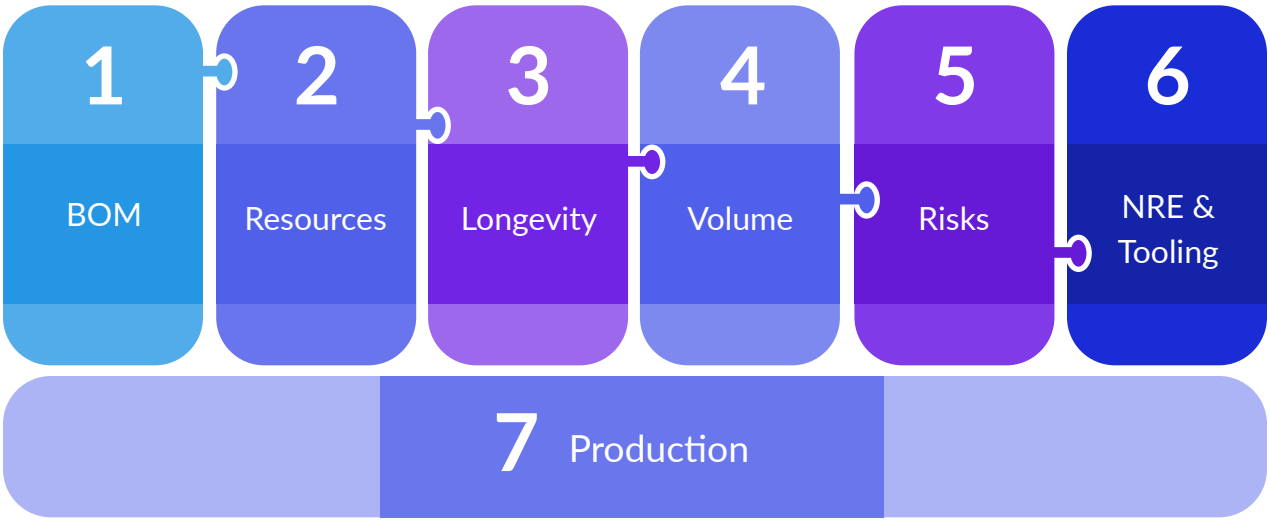
So, what if you need to make a design change midway through the ASIC development process? After all, things go wrong and requirements often change unexpectedly. Be proactive and make sure both you and your analog ASIC supplier understand this and have a corrective action plan in place. Keep in mind that there may be additional charges involved, depending on the changes requested and how far along the design is.

In the ASIC world, this is where analog differs greatly from digital, where parametric performance is almost a no-brainer. In digital, every function that connects to another function has a well-defined interface. It's either a logic 1 or a logic 0, and each of these has a well-defined minimum and maximum limit. Conversely, analog design requires that thousands, possibly tens or hundreds of thousands, of device interconnects on the chip match exactly.

For NRE, this means that when specifying and designing analog ASICs, there is significantly more custom engineering involved. It also means that much more care and consideration must be put into the budgetary proposal being prepared for the customer. It's not unusual for a back-and-forth technical Q&A to take place between the lead ASIC designer and the customer's point person. The ASIC supplier needs to know everything there is to know about the design: its application, environment, architecture, and more. This process of thoroughly understanding the customer's needs can take weeks — sometimes months — before a legitimate proposal can be offered.

And while the ASIC design manager is evaluating the basic ASIC itself, another ASIC team is looking into how this chip is going to be tested. They need to know the levels of precision required; which power management blocks are involved; if there any special noise, power-up, or high-voltage requirements; whether or not a special analog tester needs to be designed and built; and much more.

The cost of NRE and tooling can vary greatly. Variables include the design complexity, as reflected in: the labor required to design and layout the chip; mask costs, which are determined primarily by the lithography of the wafer process; wafer costs that are determined in part by the wafer size; and special needs such as number of layers, SOI, cavity etch for sensors, and more. Your analog ASIC supplier will review with you any options and tradeoffs available that might help minimize these costs.



Supporting all of these puzzle pieces is production capability. During the proposal development phase, the ASIC design team investigates the wafer fabrication processes that are suitable to produce your design, selecting the one they feel is the best solution. The IC will be designed to meet the specific requirements of this silicon process. With rare exception, silicon fab processes cannot be changed or modified.

The burden is 100% on the ASIC design team to get it right. If you remember only one thing from this paper, let it be to NEVER SEPARATE DESIGN FROM PRODUCTION. Doing so sets the stage for conflict when something goes wrong.

Unless your analog ASIC supplier is developing or modifying a process, when a performance issue arises in the initial silicon samples, 99 times out of 100 it will be a design problem. Yet independent analog design houses will argue the contrary, and you, the customer, are stuck in the middle. This is not where you want to be. Even if you have lots of experience managing the backend for digital ASICs, you should always use a full-service or turn-key supplier for analog ASICs.

Unlike digital ASICs, analog designs are extremely difficult (dare I say impossible?) to port to a fabrication process other than the one they were originally designed for without doing a major redesign or re-layout of the chip. For this reason, selection of a reputable foundry, one with a solid track record of analog IC production, is paramount. During the chip's design phase, the ASIC design team also considers the longevity of the process being selected. Is it well established with proven reliability? Does the foundry have considerable volume running on this process, reducing its likelihood of being discontinued to zero? Answering these questions helps you to mitigate the risks.

During the feasibility study period, a detailed specification of the IC is generated. This specification is similar to a typical semiconductor datasheet in terms of its contents. There may be a brief description of the IC and a definition of the maximum operating limits (temperature, voltage, etc.), followed by a detailed electrical specification. The accuracy and completeness of the electrical specification is critical, because it's used to define accept/reject criteria for the ASIC. The electrical specification becomes a part of the development contract, usually as one of several "Exhibits" attached at the end. It is not unusual for minor changes to be made to the electrical specification (but only by mutual agreement) during the development of the chip, if one side or the other notices things that may be mutually exclusive or discovers a means by which the chip can be further improved or reduced in size.

When the electrical specification is finalized and the contract is signed, development begins. Weekly, sometimes daily, discussions between the ASIC supplier and customer keep both sides in synchronicity throughout the development period. Periodic milestone reviews are held as well as a final signoff review, at which point the design is declared finished and the hard tooling / wafer fabrication phase begins.

Once the foundry has produced the masks, they will begin wafer production. Throughput can vary from 16 to 24 weeks before a finished wafer is delivered back to the ASIC supplier for testing. If all goes according to plan, the ASIC supplier will have the test system finished and awaiting wafers to test. Thanks to the skills of experienced analog design engineers, 99% of designs are fully functional in this first look. However, with analog, almost all designs will require minor tweaks to achieve complete parametric compliance with the specification — it's just the nature of the beast. Although analog design and verification tools continue to improve, none are perfect. Still, a lot can be learned from a functional part. Samples are prepared and sent to the customer for evaluation. Any nonconformities or performance nuances are noted and normally corrected with a minor tweak to the metal layers of the chip. Upon verification by the customer, the revised chip is released to production.

Advance planning, thoughtful and proper resource allocation, an intimate understanding of your supplier's analog design and production skills, and a well-defined objective specification will ensure the success of your project.

A couple of side notes to keep in mind:

1 When it comes to analog, there are no shortcuts. If you insist on shorter and shorter development times from your supplier, it may backfire on you. Although delivery of first samples sometimes occurs in as little as 10 months, realistically you should expect it to be closer to 12 to 15 months or longer for very complicated designs. Individual quotes will vary.

2 Think about your intellectual property (IP). If your design is simply an amalgamation of off-the-shelf standard products with no inherent invention in the design, you may not care. But if the chip contains your own proprietary IP, check very carefully as to where your chip will be designed. Yes, engineers in the U.S. and EU may be more costly, but what are the costs to you and your business if your design is stolen? Have you ever wondered how products become available for sale on Alibaba before being released by their brand-name manufacturers?

The same holds true for wafer fabrication. If you are at all concerned, insist that the product be fabricated where the rules of international law apply.

3 Don't be pennywise and pound foolish. When having an analog ASIC made for you, be very thorough about whom you select to design and build it. The cheapest solution may not be the best.

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